

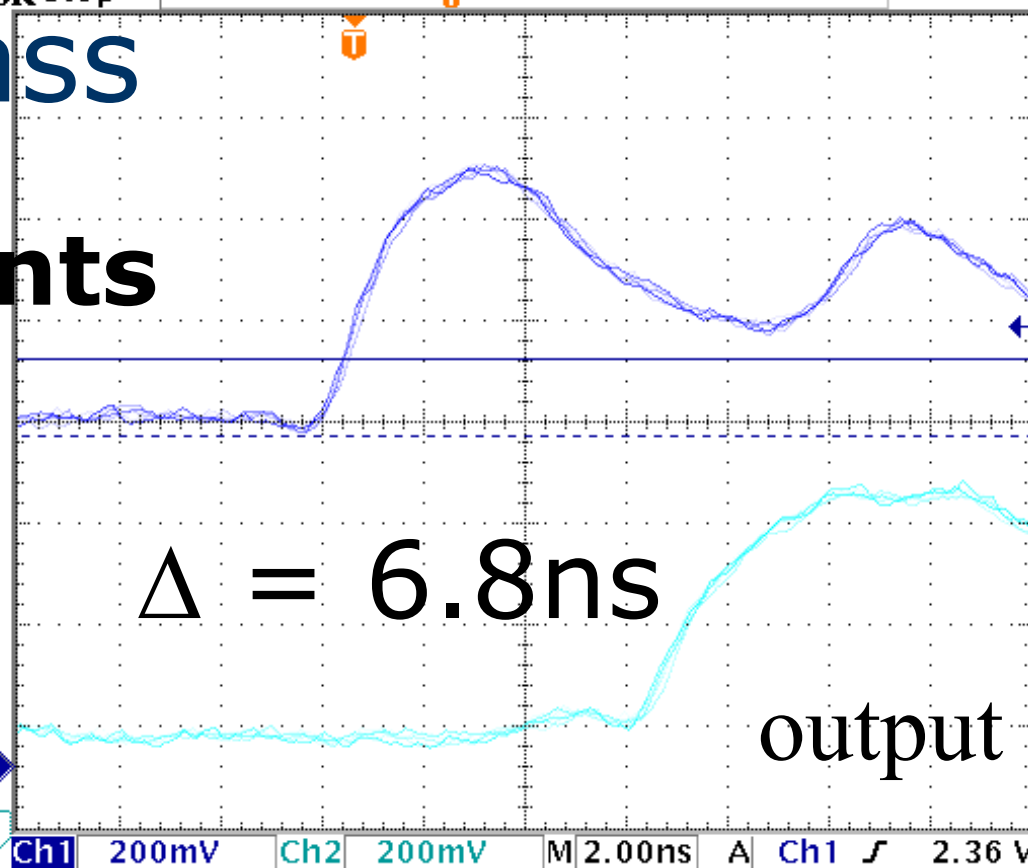
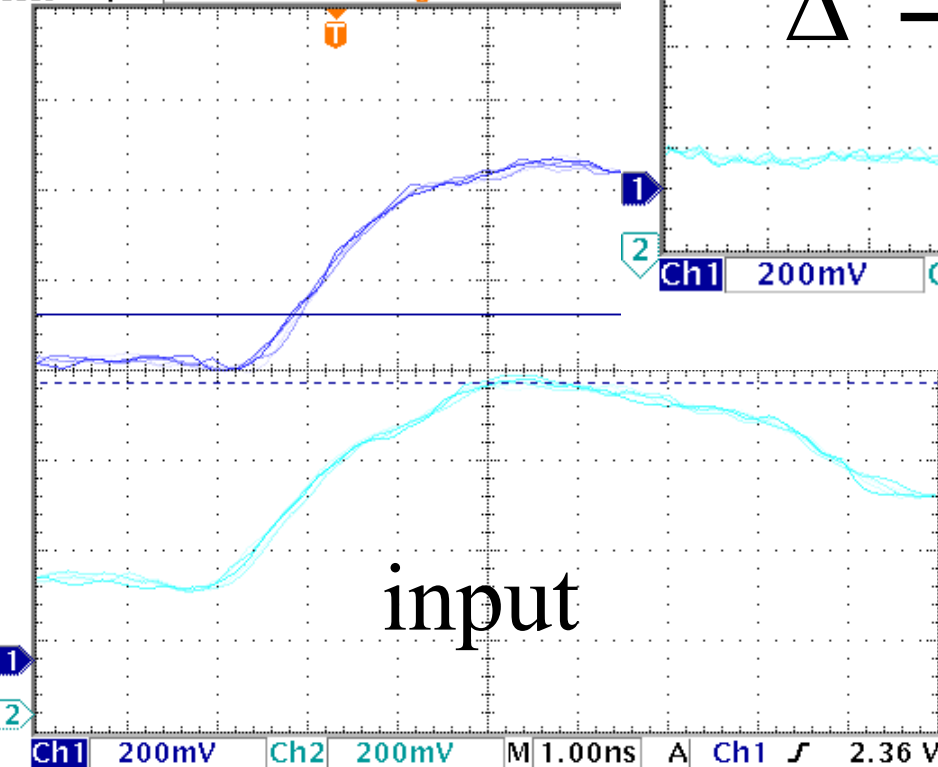
Full Chain Status

S.Burdin

Clock Bypass

Measurements on AC

Tek Stop



$$\Delta = 6.8\text{ns}$$

Δ: 152mV
@: 2.30 V

Ch1 High
2.40 V

Ch2 High
1.49 V

Ch1→Ch2↗↘→
6.771ns

33.20 %

Ch2 High
2.62 V

Ch1→Ch2↗↘→
-97.16ps
Low
resolution

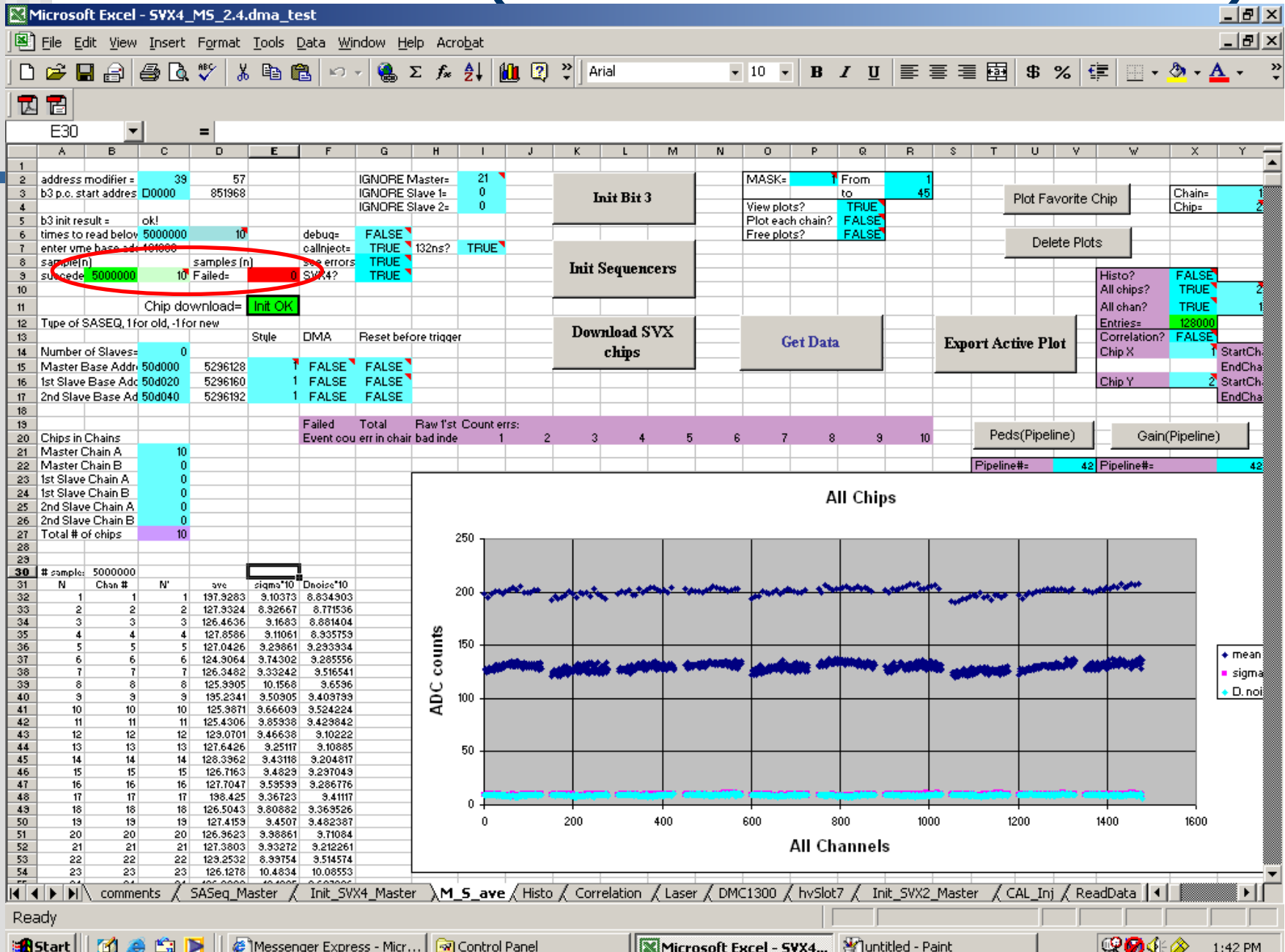
Cable was
added to
compensate

11 Mar 2003
14:04:59

33.20 %

11 Mar 2003
14:14:45

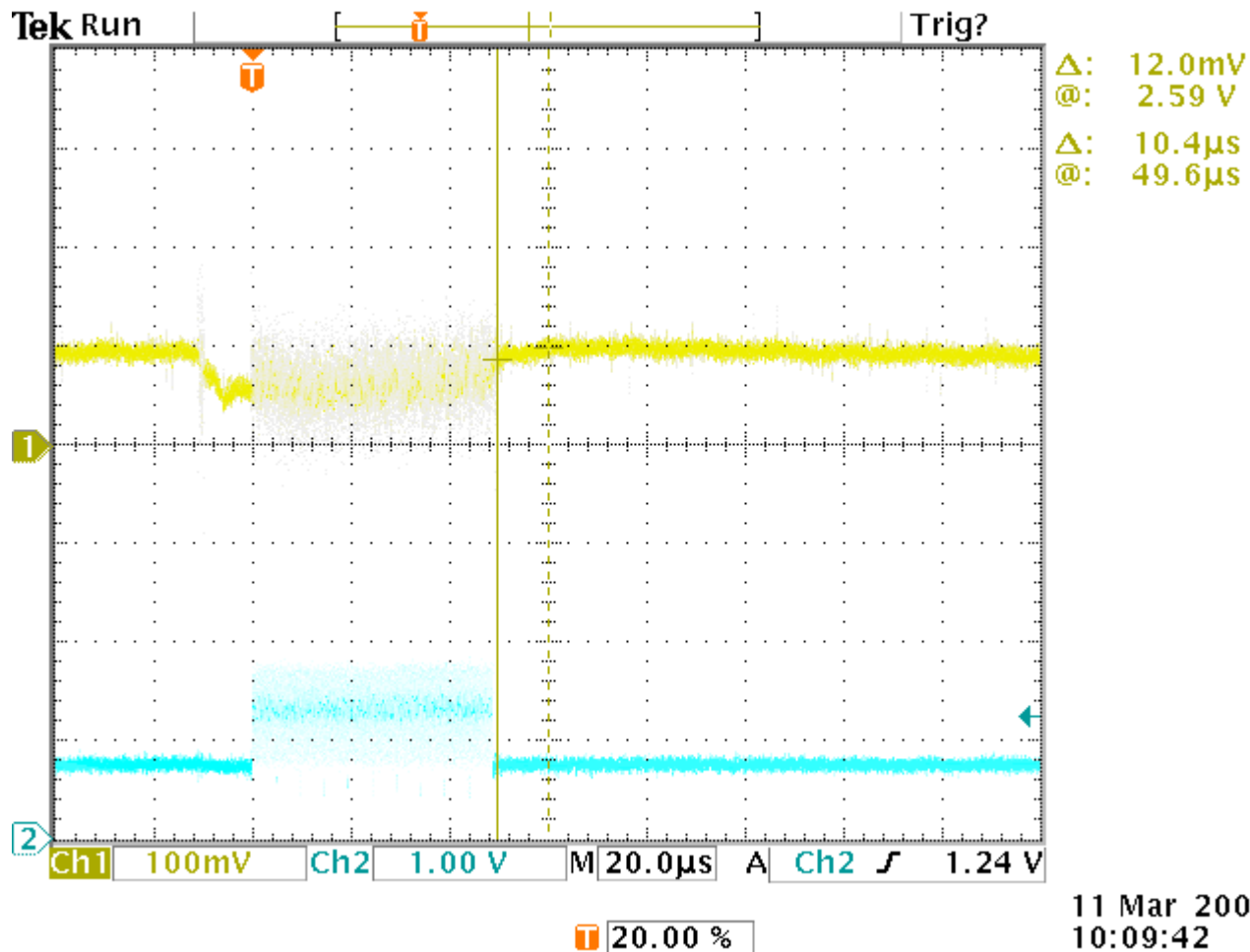
Worked Fine (5M Events Passed)



Voltage Measurements

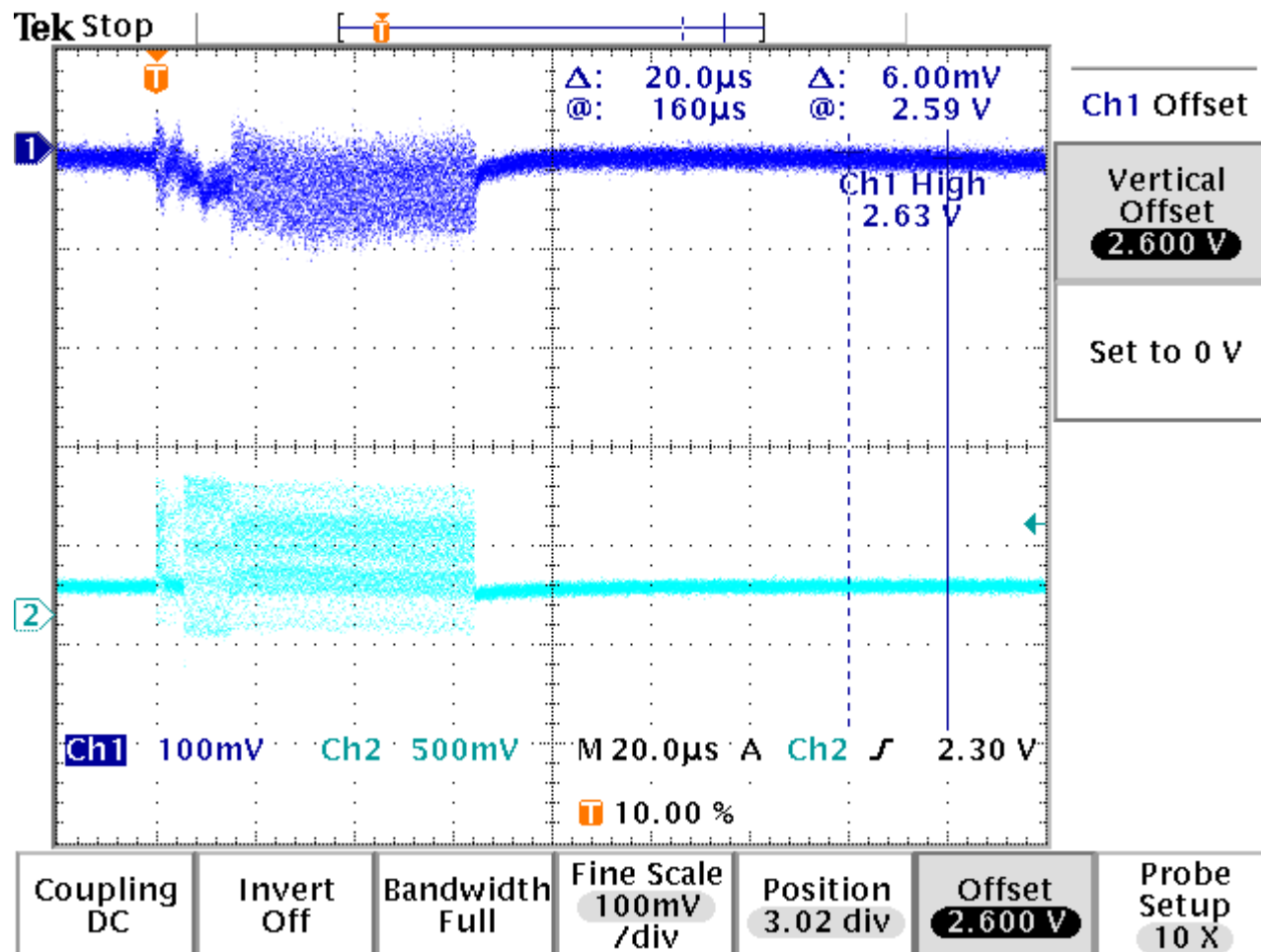
- Russell's setup
- But
 - The original capacitor on AC
 - Measurements are on the hybrid

Picture From Russell

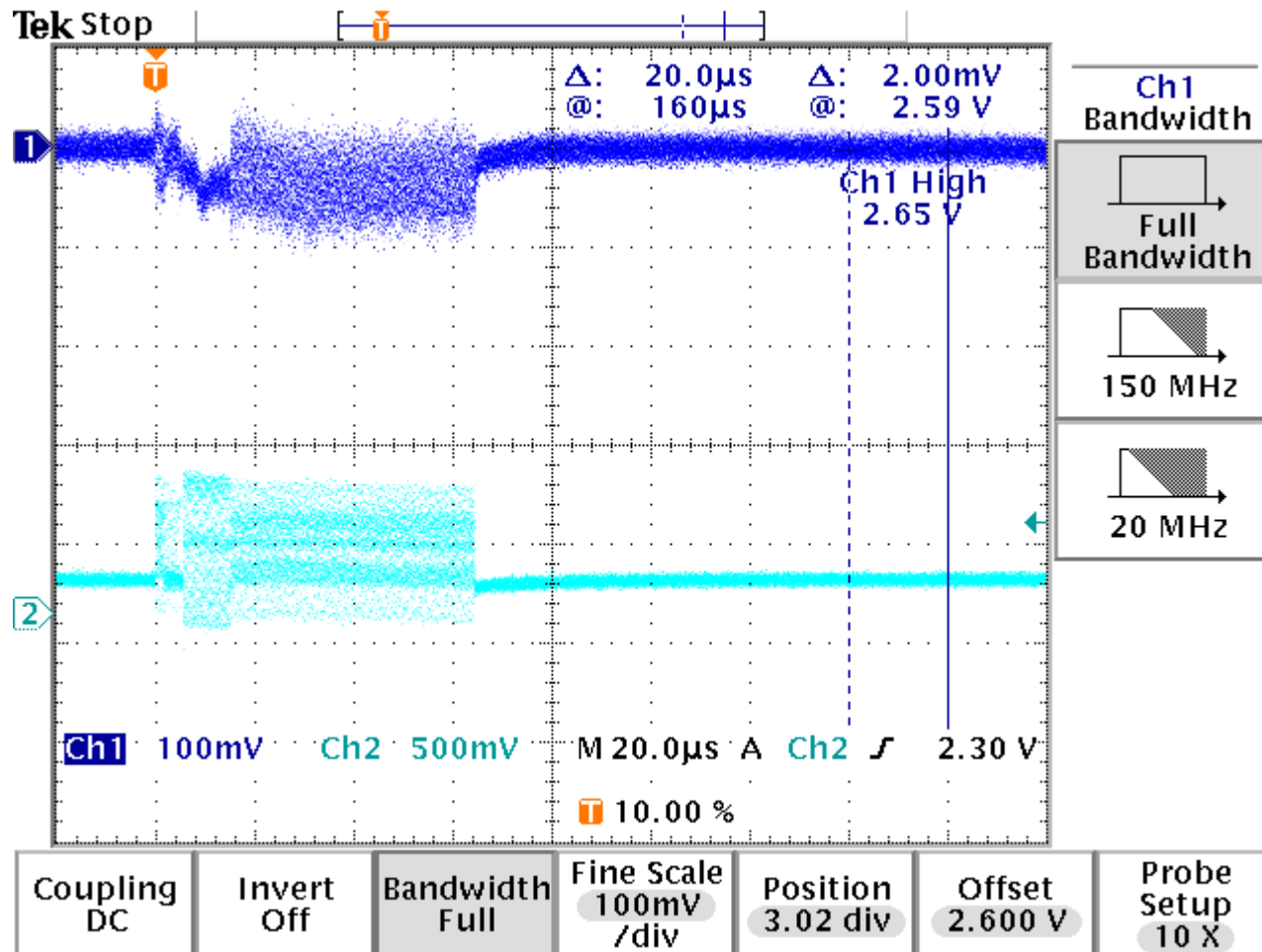


11 Mar 2003
10:09:42

VDD Measurement on the Hybrid

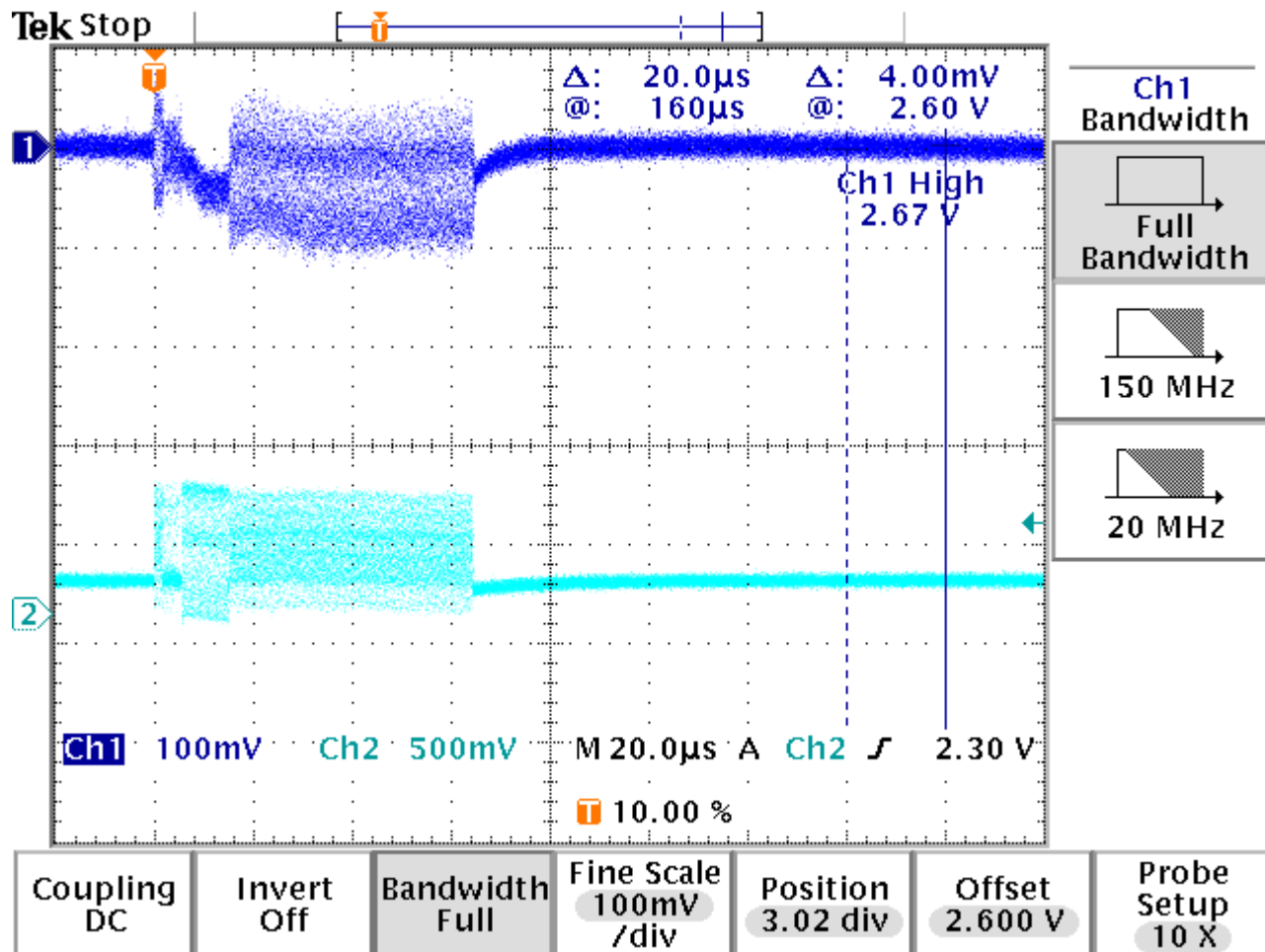


AVDD & DVDD Are Shortened on Hybrid Also



Full Chain stopped
to work (no download).
Work resumed only after
removing the additional cable
from the clock lines

Additional 10 μ F on Hybrid



Conclusion

- VDD behavior in SiDet is close to the one in KSU
- 10 μ F on Hybrid added some small tail in VDD
- Additional study is needed on the clock bypass